IN THE CLAIMS

Please amend the claims as shown below.

1. (Currently Amended) A high voltage device formed in a region of a silicon substrate of a first conductivity type delimited by a wall of a second conductivity type, comprising:

a lower surface comprising a first region of the second conductivity type connected to the wall.

an upper surface comprising a second region of the second conductivity type,

a high voltage being likely to exist between the first and second regions and having to be withstood on the upper surface side by a junction between the second region and the substrate or by a junction between the wall and the substrate,

a conductive track being likely to be at a high potential extending over the substrate between the second region and the wall, and

a third region of the first conductivity type of a high doping level formed in the substrate under a portion of the track substantially halfway between the second region and the internal periphery of the wall, the third region being contacted by a field plate which is insulated from the track, and extends widthwise at least substantially across the track and lengthwise beyond the third region on either side of the third region in the direction of the wall and of the second region.

2. (Previously Amended) The device of claim 1, wherein the field plate extends beyond the third region in the wall direction and in the direction of the second region over a distance greater than 10 μm.

3. (Previously Amended) The device of claim 1, wherein the external periphery of the second region comprises a ring of the same conductivity type as the second region, but having a lower doping level than the second region.

4. (Currently Amended) A high voltage device formed in a region of a silicon substrate of a first conductivity type delimited by a wall of a second conductivity type, comprising:

a lower surface comprising a first region of the second conductivity type connected to the wall;

an upper surface comprising a second region of the second conductivity type;

a conductive track extending over the silicon substrate between the second region and the wall;

a third region of the first conductivity type having a high doping level formed in the substrate under a portion of the conductive track approximately halfway between the second region and an internal periphery of the wall; and

a field plate which is insulated from the track and extends widthwise at least substantially across the track and lengthwise on either side of the third region, beyond the third region, in the direction of the wall and of the second region, at least a portion of the field plate being in contact with the third region.

extending the field plate to the right of N^+ region 35 would not improve the ohmic contact of the structure, since a good ohmic contact is not formed by contacting a conductive layer to the lightly doped N-type substrate. Thus, there is no reason taught or even suggested by Whitney to have the field plate extend to the right of N^+ region 35.

During the telephone interview the Examiner also commented that he did not see a reason for allowance of the present application since the figures of the present application are similar to the figures in Whitney. This, however, is not relevant. When determining patentability, it is necessary to compare the claimed invention to the teaching of the references. It is improper to deem claims unpatentable due to perceived similarities between the figures of an application and the references.

While no agreement as to the allowability of the claims was reached, or as to any manner by which to amend the claims in order to place them in condition for allowance, the Examiner did indicate that the claims would distinguish over the combination of Whitney and Applicant's admitted prior art if he were convinced that the field plate 31 of Whitney does not extend lengthwise beyond region 35 on either side of region 35.

Claims 1-4 Distinguish Over the Combination of Whitney and Applicant's Admitted Prior Art

Claim 1

Claim 1 is directed to a high voltage device formed in a region of a silicon substrate of a first conductivity type delimited by a wall of a second conductivity type. The high voltage device comprises a lower surface comprising a first region of the second conductivity type connected to the wall, an upper surface comprising a second region of the second conductivity type, a high voltage being likely to exist between the first and second regions and having to be withstood on the upper surface side by a junction between the second region and the substrate or by a junction between the wall and the substrate. The high voltage device further comprises a conductive track being likely to be at a high potential extending over the substrate between the second region and the wall, and a third region of the first conductivity type of a high doping level formed in the substrate under a portion of the track substantially halfway between the second region and the internal periphery of the wall, the third region being contacted by a field plate